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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/817,630	04/02/2004	Robert E. Cypher	5181-98801	2867

35690 7590 03/02/2007

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EXAMINER	
DOAN, DUC T	
ART UNIT	**PAPER NUMBER**
2188	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	03/02/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/817,630	CYPHER ET AL.	
	Examiner	Art Unit	
	Duc T. Doan	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 January 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5,7-10,12,13 and 15* is/are rejected.

7)☒ Claim(s) *6,11,14,16-17* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Status of Claims

Claims 1-17 have been presented for examination in this application. In response to the last office action, none of claims have been amended, none of claims 11,19,27 have been canceled. As the result, claims 1-17 are pending in this application.

Applicant's remarks filed 1/27/07 have been fully considered but they are but they are mooted in view of new ground(s) of rejection by Examiner.

Claims 1-5,7-10,12-13,15 are rejected.

Claims 6,11,14,16-17 are objected to.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

A person shall be entitled to a patent unless -

(a) the invention was known or used by other's in this country or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in a patent granted on an application for patent by another fled in the United States before the invention thereof by the applicant for patent, or on an international application by another

who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

Claims 1-5,7,9-10,12-13,15 are rejected under 35 U.S.C. 102 (b) as being anticipated by Chi et al (US 5940870).

As in claim 1, Chi discloses a system, comprising: a plurality of nodes, wherein each node comprises an active device and a memory subsystem coupled to the active device (Chi's Fig 4 show a node having memory subsystem #42-44, #42 processors); wherein an active device included in one of the plurality of nodes includes a memory management unit configured to receive a virtual address generated within that active device and to responsively output a global address identifying a coherency unit, wherein a portion of the global address identifying a translation function (Chi's Fig 4: #42 processor; #54 cluster cache and directory; Fig 8: a memory management unit received virtual address generated from/within the processor the cluster, translates to a global address on interconnect; a portion of global address #110 identify the translation function; a portion of global address identifying a coherency unit (memories in the node), with Fig 8: 114 node ID, #110 partition ID),

wherein the memory subsystem included in the node is configured to perform the translation function identified by the portion of the global address on an additional portion of the global address in order to obtain a local physical address of the coherency unit (Chi's Fig 7, column 6 lines 21-35 discloses the processor at the destination node is configured to perform the translation function identified by Fig 8: #110 logical partition (corresponding to the claim's "portion of the global address on an additional portion of the global address") in order to obtain a local physical address of the coherency unit (Fig 7, column 5 lines 1-10, discloses translation of

physical to global memory space when sending the packet, and translation from global memory space to local space when a packet is received at the destination node),

wherein each active device included in the node is configured to use the portion of the global address identifying the translation function when determining whether a local copy of the coherency unit is currently stored in a cache associated with that active device (Chi's Fig 7, column 1-10 discloses each processor determine if data is in its memory "local space").

As in claim 2, Chi's Fig 8, column 27-47 discloses the bits of logical partition number #110 and ATM index bits are used to identify the "global memory space", which is duplicated and shared in coherency memories of multiple nodes (Chi's column 2 lines 1-21).

As in claim 3, Chi discloses if the at least one bit included in a different global address indicates that the different global address is not replicable in more than one of the plurality of nodes (Chi's Fig 8 discloses if the bits of the partition number does not indicate that the global address in the shared/replicable global address space), the portion of the different global address includes additional address bits instead of identifying a translation function (Chi's Fig 8 discloses that a potion of the global address includes additional address bits such as offset #104).

As in claim 4, Chi discloses wherein the additional portion of the global address for the coherency unit generated by each active device in the plurality of nodes has a same value, and wherein active devices in different nodes of the plurality of nodes generate different values of the portion of the global address identifying the translation function. Chi's column 5 lines 40-50 discloses the partition number #110 is the logical node ID for applications running in the processors, these logical partitions in nodes can have the same values, for example for private and "near global memory", they have the same partition number zero (see column 6 lines 20-36).

As in claim 5, Chi discloses a home memory subsystem included in a home node of the plurality of nodes for the coherency unit is configured to store the portion of the global address identifying the translation function for the node (Chi's Fig 8 discloses the source nod/home node is configured to store a portion of global address such as partition number that identifying the translation function associating with the node), wherein active devices included in the home node are configured to generate a different value of the portion of the global address (Chi's Fig 8 discloses the processor in the home node/source node are configured to generate a different values of the partition number which is a portion of the global address), wherein the different value identifies a different translation function associated with the coherency unit in the home node (Chi's Fig 7, column 6 lines 1-10 further discloses the portion of global address having different values to access different near global space portions or global space portions in the shared distributed memories in a coherency manner).

As in claim 7, Chi discloses the active device included in the node is configured to output the global address in an address packet on an address network coupling the active device to an additional active device within the node in order to initiate a coherency transaction for a coherency unit identified by the global address (Chi's Fig 7, column 6 lines 1-10 further discloses several processors in multiple nodes are configured to initiating and receiving address packet in a coherency manner).

Claim 9 rejected based on the same rationale as of claim 1.

Claim 10 rejected based on the same rationale as in the rejection of claim 2.

Claim 12 rejected based on the same rationale as in the rejection of claim 4.

Claim 13 rejected based on the same rationale as in the rejection of claim 5.

Claim 15 rejected based on the same rationale as in the rejection of claim 7.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chi et al (US 5940870), in view of Arimili et al (US 2002/0112124).

As in claim 8, the claim recites wherein a memory controller included in the memory subsystem is integrated in a same integrated circuit as the active device. Chi does not describe the claim's aspect of integrated memory controller. However, Arimilli's paragraph 6 discloses a multiple processors system with integrated memory controller circuit. It would have been obvious to one of ordinary skill in the art at the time of invention to include integrated memory controller circuit as suggested by Arimilli in Chi's system to allow fast communication between the processor and the memory controller since they are located in the same chip (Arimilli's page 1 paragraph 6).

Allowable Subject Matter

Claims 6,11,14,16-17 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

Applicant's arguments filed 1/27/2007 have been fully considered with the results as follows,

A) Regarding the arguments on pages 2-4 for the rejections of claims 1,9 under 35 U.S.C. 102 (b),

Applicant argues on page 3 last paragraph to page 4 first paragraph that Chi does not teach the claim 1's limitation of "a portion of the global address identifying a translation function". Examiner respectfully disagrees. Chi teaches a translation function that is translating addresses between global address space and local address spaces of memories being shared in a multi processor clustering system (see Chi's Fig 7, translation function between a global memory address space and destination node's local address space). In order to carrying out **this address translation function in each node,** it requires translation information such as Fig 8: #114 node ID, #110 partition number **in the global address** Fig 8: #112, to identify the translation function that is identifying translating function from an address in global address space into local address space (see Chi's Fig 7, global memory address space, private memory address space, near global memory address space etc..). Thus Chi teaches the claim's limitation of "portion of the global address identifies a translation function".

Chi's Fig 8 further teaches the actions to perform the address translation function (corresponding to the claim's "performing a translation function in response o the translation information"), for example looking up the ATM address mapping table in order to obtain the translated address (see Chi's column 5 lines 28-35).

Chi further discloses that active device in each node is configured to use the information in the global address identifying the translation function when determining a local copy of the coherency unit is currently stored in a cache associated with that active device (Chi's Fig 7, column 5 lines 1-10 discloses that the processor in each node of a cluster determines whether the address is associated with local address space or is associated with a global address space (i.e a copy of data is stored in the local copy of the global address space, Fig 7: #98) which is a shared coherency address space among the processors in the cluster.

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Applicant's arguments filed 1/27/2007 have been fully considered with the results as follows,

A) Regarding the arguments on pages 2-4 for the rejections of claims 1,9 under 35 U.S.C. 102 (b),

Applicant argues on page 3 last paragraph to page 4 first paragraph that Chi does not teach the claim 1's limitation of "a portion of the global address identifying a translation function". Examiner respectfully disagrees. Chi teaches a translation function that is translating addresses between global address space and local address spaces of memories being shared in a multi processor clustering system (see Chi's Fig 7, translation function between a global memory

address space and destination node's local address space). In order to carrying out **this address translation function in each node,** it requires translation information such as Fig 8: #114 node ID, #110 partition number **in the global address** Fig 8: #112, to identify the translation function that is identifying translating function from an address in global address space into local address space (see Chi's Fig 7, global memory address space, private memory address space, near global memory address space etc..). Thus Chi teaches the claim's limitation of "portion of the global address identifies a translation function".

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Conclusion

When responding to the office action, Applicant is advised to provide the examiner with the line numbers and page numbers in the application and/or references cited to assist examiner to locate the appropriate paragraphs.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Duc T. Doan whose telephone number is 571-272-4171. The examiner can normally be reached on M-F 8:00 AM 05:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hyung S. Sough can be reached on 571-272-6799. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Duc Doan
Patent Examiner
Art Unit 2188

Hyung S. Sough
Supervisory Patent Examiner
Art Unit 2188

3-1-07